The Control System Design for 600kV High Voltage Platform of HIAF Electron Cooler

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ABSTRACT

HIAF is the next generation heavy ion accelerator in China, it contains lots of sub facilities. The electron cooler is one of the most significant facilities in HIAF of Spectrometer Ring (SRing). With the electron cooler, SRing could generate high quality and high intensity ion beam for the experiments. The electron cooler in HIAF was designed to produce 600KeV electron beam. To achieve this design target, high voltage needs to reach 600kV maximum and ripple wave less than 1*10-4. A new control system was designed for the high voltage platform which uses cascaded transformer construction. The system makes use of XGS-PON network as the main means of communication. Zynq 7015 as the CPU of the embedded controller. The controller integrated 2 DAC ports with 100KS/S and 4 ADC ports with 200KS/S for high voltage modules setting and high voltage divider monitor, 8 low-speed ADC ports for auxiliary power supplies, and the environment sensors. The embedded Ubuntu Linux and the EPICS frameworks were programmed in the controller, all of the control parameters were sent through channel access protocol. No need for host computer to participate in control logic, only used for display. The hardware mentioned above interacts with the operating system through the FPGA part of Zynq. The FPGA is programed as a coprocessor for communicating, data processing and interlock control. Corresponding drivers are integrated in the Linux system at the same time.

CCS CONCEPTS

• **Applied computing**; • **Physical sciences and engineering**; • **Physics**;

KEYWORDS

HIAF, Electron cooler, Accelerator, Embedded controller, Control system, XGS-PON, Zynq

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1 INTRODUCTION

Electron cooler[1] is the main facility for SRing beams cooling of HIAF[2]. The Coulomb collision between electron beam and ion beam could be used to reduce the transverse energy of ion beam and improve the beam quality. And the same time, the electron cooler can also be linked with the electron target experimental terminal[3], so as to improve the energy scanning range of the electron target experimental terminal and expand the experimental range. The electronic cooler is designed to generate an electron beam of up to 600KeV.

In order to achieve the design goals, a special control system for the special high voltage platform is needed. The high voltage platform is special because the power supply needs to capable of generating 600kV voltage maximum with a ripple of less than $1*10^{-4}$ which makes sure the electron beam could keep in a specific energy state. Due to the characteristics of the voltage doubling circuit, the ripple of ordinary high voltage power supply can only reach $1*10^{-2}$, and the output current is also tiny.

To solve those problems, a new high voltage power supply has been designed, which is mainly composed of 15 cascading transformers in series with a group of high voltage modules respectively. Each group consists of a positive 20kV and a negative 20kV high voltage module to form a 40kV module. The front stage of the cascading transformer adopts a 20kHz high-frequency AC power supply. Since the electron gun is a capacitive load, the ripple generated by high frequency power supply can be further suppressed by fine-tuning the capacitance of the entire load.

The output voltage of the whole high voltage power supply can be adjusted by controlling the output voltage of each group of high

voltage modules. Since the high voltage modules of each group are at different potentials, there are a large number of auxiliary power sources, and conditions in the modules of each group that need to be monitored, which is much more complicated than the traditional high voltage power supply. At present, the authority in this field of study is Budker Institute of Nuclear Physics[4], the main control method is the ZigBee+STM32 technical solution. The solution has some disadvantages in practical application as follows:
The speed of ZigBee communication mode is slow, and big data such as voltage waveform data cannot be transmitted.
When there are multiple nodes in the ZigBee network, the GTS protocol is used to communicate with each node in turn, and the cycle of traversing all nodes is very long more than 10 seconds.
The ZigBee antenna needs to leave a separate gap on the voltage equalizing ring of each high voltage module group, so as to ensure that the wireless signal can be sent and received normally. However, the voltage equalizing ring is destroyed to some extent, which may lead to the tip discharge phenomenon when the high voltage is rapidly adjusted.
The Zigbee base station needs to be placed in the SF6 tank, which is easily affected by high voltage.
Traditional STM32 chip is lacks MMU, which can only control simple IO and cannot run operating system to finish the complex tasks.
The protocol which they used is private, cannot directly connect to the accelerator's main control system.

In order to solve the above problems, this paper designs a new control structure using XGS-PON network[5] as the main communication network, and Zynq 7015[6] as the main control chip for each high voltage module, which integrates ARM A9 and FPGA simultaneously. This system runs Linux operating system in ARM and develops an IOC program to deal with high voltage logic and remote control instructions based on EPICS framework[7]. On the other hand, digital and analog signal processing logic is put into FPGA part, and data interaction with ARM is carried out through DMA channel.

2 SYSTEM DESIGN

The overall system structure is shown in figure 1. The main high voltage device is located in the sealed tank of SF6. The high-pressure tank is connected with the external OLT[8] through a single optical fiber, and a splitter is used inside the high-pressure tank to connect the main control board of the 15-group control unit.
The control structure of each group of high voltage modules is shown in figure 2. In the one group of modules, there are three auxiliary power supplies, which respectively supply power to the analog signal board, main control board, and the high voltage module. The purpose of the separate power supply is to prevent the high voltage from affecting the equipment along the power supply line during the high voltage discharge. Outside the main control board, there is a fast-analog signal board, a slow analog signal board, and an environmental sensor board. The fast-analog signal board is mainly used for the control of the 40kV high voltage module. It has four ADC channels for voltage and leakage current monitoring and two DAC channels for voltage setting. The slow analog signal board is used to monitor the state of various auxiliary power supplies.

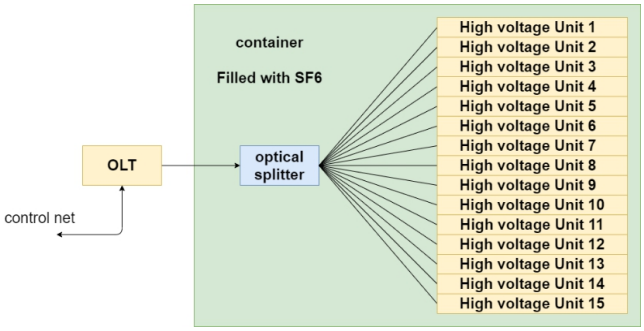

Figure 1: System Architecture.

When high voltage discharge occurs, the auxiliary power supply may be damaged. The slow analog signal board can be used to assist in fault diagnosis. The environmental sensor board monitors the pressure and temperature in the tank, usually keeping SF6 around 2MPa.

Inside the control board, there are two parts of Zynq. One is FPGA and the other is ARM. The FPGA is programed as a coprocessor, it is responsible for all communication with external equipment such as DAC, ADC, network device, sensor and processing control signals of the operating system. ARM is used for running Linux system.

In the FPGA part, there are four area for different function. The first is communication function area. In order to communicate with XGS-PON network, a dedicated fiber chip must be needed. We use 1G ethernet SGMII IP core and some peripheral logic to finish those function. The second is DAC function area, this function need to serial output the digital signal to the DAC chip, the characteristics of the serial cause the clock bus to run at 10MHz. the third is ADC function area, there are four high speed simultaneous ADC channels, and the signal also was transferred in serial mode. The difficulty in this area is that realize continuous data collection in a limited buffer without point loss. The realization of this function requires the collaborative design of FPGA and system driver. DMA channel and ARM's interrupt are used to achieve lossless data collection. The last is sensor process function area, the sensor chip use IIC bus to upload the environment data, so an IIC controller is built in this area.
In the ARM part, an embedded Ubuntu Linux operating system is built, the system supports complete Ubuntu functions except for the graphical interface. With the gcc, make and apt-get commands, the programmer could build the program directly in the controller without cross complier environment. All the hardware can be found in the /dev directory. In the operating system, an IOC program which based on the EPICS framework is built. With the EPICS framework. All variables are accessed and controlled through Channel Access protocol, including voltage setting and monitoring, leakage current, auxiliary power supply, SF6 pressure, temperature and other variables, 52 variables in total. In the IOC program, many kinds of records are used to generate the real-time data including analog input record, analog output record, analog array input record, calcout record (calculation output record), compress record etc. At the same time, the software PID algorithm is integrated to fine-tune

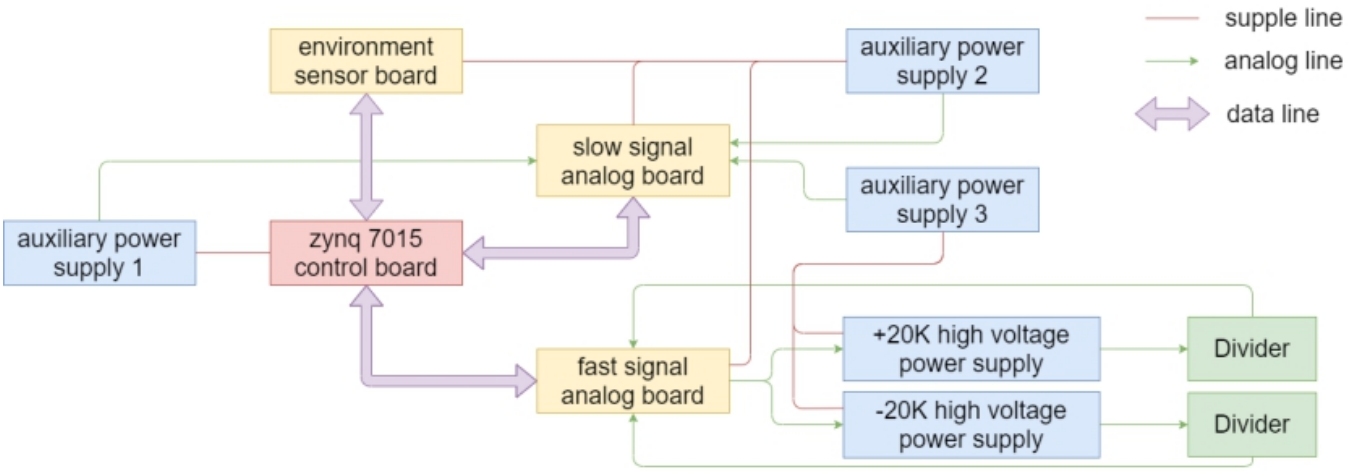

Figure 2: Control Structure of the Unit.

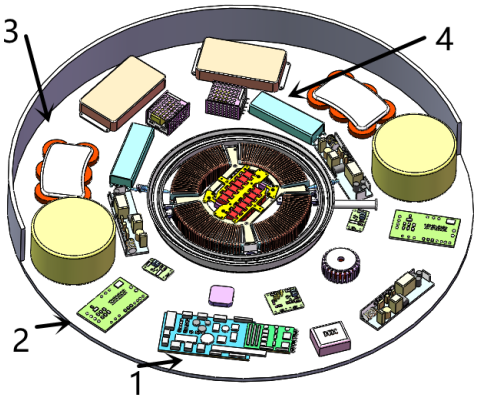

Figure 3: Assembled 40kV Module.

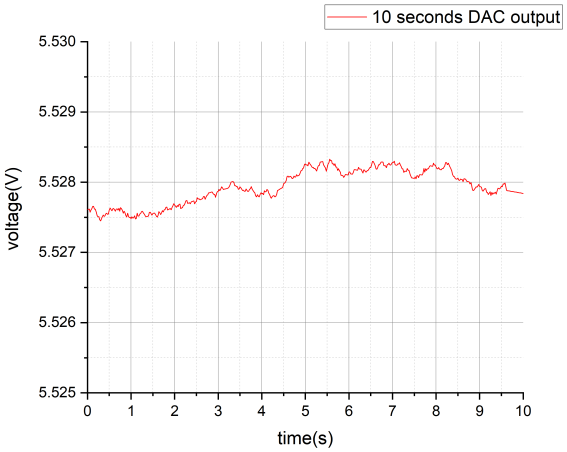

Figure 4: Short-Term Dac Output Measure.

the accuracy and long-term stability of the high voltage module in real time. The algorithm is also encapsulated in the program.

Based on our design, the 3D assembly diagram of the single-group module in shown in figure 3. The communication fiber is plugged into the control board which is board number 1, the cylindrical modules are high-precision voltage dividers, the boards number 2 which behind the dividers are measurement calibration circuits. The control system collects accurate high voltage information from it. The modules number 3 are high voltage filter capacitor and number 4 are ±20KV high voltage generator. The middle of the picture shows the cascaded transformer. All the power supply to the superior group and this group comes from here.

3 EXPERIMENT

Based on the overall requirements of the system, the output of the high voltage system is mainly affected by the stability of the DAC in the control system side.

We conducted short-term and long-term stability tests on the DAC output of the control system. The short-term test results are shown in figure 4. The output ripple of DAC itself can be seen from the short-term stability. As can be seen from the figure, DAC fluctuation in the short term is about 0.0015V, the total output is ±20V, so the relative ripple is $7.5*10^{-5}$, which meets the design requirements.

Long-term test results are shown in figure 5, because the data is very huge from the high-speed ADC channel, it was compressed and averaged. From the figure it can be seen that the DAC output basically changes periodically within a certain range. May be affected by ambient temperature. In the future, the software PID algorithm will be dynamically corrected according to the data from the divider.

For an embedded controller, another important performance index is the long-term operating device temperature and CPU usage. The temperature decides the controller's long-term operation life and stability. A temperature sensor is integrated in the Zynq chip. After testing, the temperature of the controller in the air can be kept

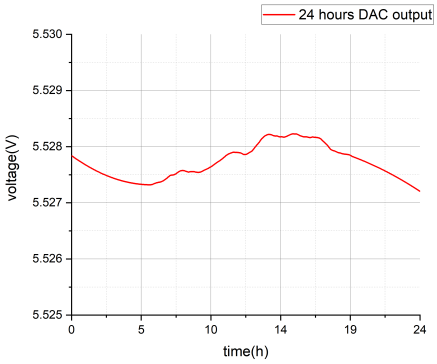

Figure 5: Long-Term Dac Output Measure.

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top - 17:00:10 up 6 days, 55 min,  2 users,  load average: 0.25, 0.22, 0.19
Tasks:  62 total,   1 running,  38 sleeping,   0 stopped,   0 zombie
%Cpu(s):  0.9 us,  1.0 sy,  0.0 ni, 98.1 id,  0.0 wa,  0.0 hi,  0.0 si,  0.0 st
KiB Mem :  1030120 total,   847576 free,    47436 used,   135108 buff/cache
KiB Swap:        0 total,        0 free,        0 used.   906376 avail Mem

  PID USER      PR  NI    VIRT    RES    SHR S  %CPU %MEM     TIME+ COMMAND
20781 root      20   0   42984  38232   4652 S   9.3  3.7   0:02.08 st.cmd
19763 root      20   0       0      0      0 D   1.3  0.0   1:54.85 kworker/1:0
20778 root      20   0    4924   2220   1832 R   0.3  0.2   0:00.06 top
    1 root      20   0    5208   3492   2576 S   0.0  0.3   0:03.27 systemd
    2 root      20   0       0      0      0 S   0.0  0.0   0:00.09 kthreadd
    4 root       0 -20       0      0      0 I   0.0  0.0   0:00.00 kworker/0:0H
    6 root       0 -20       0      0      0 I   0.0  0.0   0:00.00 mm_percpu_wq
    7 root      20   0       0      0      0 S   0.0  0.0   0:00.31 ksoftirqd/0
    8 root      20   0       0      0      0 I   0.0  0.0   0:16.69 rcu_preempt
    9 root      20   0       0      0      0 I   0.0  0.0   0:00.00 rcu_sched
   10 root      20   0       0      0      0 I   0.0  0.0   0:00.00 rcu_bh
```

Figure 6: the CPU Usage of the IOC.

below 50 degrees Celsius for a long time when it is turned on. In the SF6 tank, SF6 has a large molecular weight and a large specific heat, and its convective heat transfer capacity is better than that of air. The convective heat transfer capacity of SF6 at two atmospheric pressures is the same as that of transformer oil. Therefore, the temperature of the controller chip is lower, which further improves the stability of the controller.

Traditional embedded programs usually process each transaction one by one in a big loop, this will cause the CPU usage to always be 100% and the control chip is always running at full speed. In the IOC program which we programed, a large number of zero copy technology and semaphores are used to handle large data transmission between processes. Therefore, the CPU usage of the entire control program is extremely low as shown in figure 6, less than 10%, and memory usage only reach 3.7%. it leaves a huge space for the expansion of controller functions in the future.

According to the design of architecture, we have completed the single group assembly as shown in figure 7. The board number 1 at the left part of the figure is the control board. The board directly connected with the blue board is the fast-analog signal board. The board number 2 is the slow analog signal board and the board number 3 is mainly a rectifier circuit. Three power adapters are located below the picture. In the future, 15 group modules will be

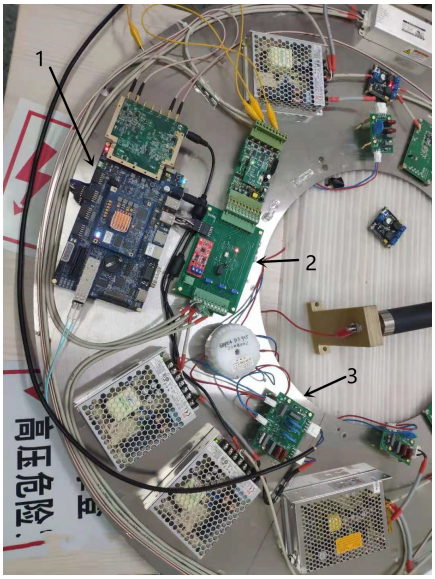

Figure 7: The Single Group of High Voltage Module.

assembled in series through cascaded transformer to achieve 600kV output voltage.

4 CONCLUSIONS

In this paper, a new control system for high voltage platform is designed including control structure and embedded controller. The new control system is compatible with this special high-voltage power supply structure. It overcomes the problem of slow communication speed at different potentials and susceptibility to high voltage. With the support of FPGA function, many high-speed circuit logics are realized by developing as IP cores, saving a lot of peripheral logic wiring. Through the embedded operating system and EPICS framework and the use of semaphore and zero-copy technology for synchronization and data exchange between threads, a large amount of CPU resources is saved, making the entire control program very efficient. Any accelerator control system can be seamlessly connected to the high voltage platform with the channel access protocol.

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